IN THE CLAIMS

This listing of claims is provided for the convenience of the Examiner; no changes are made to the claims by this Response.

Listing of Claims:

1. (Previously presented) A particularly configurable processor for processing error induced computer programs which are selectively operable on said particularly configurable processor, comprising:

a central processing unit chip;

processor circuitry on said chip;

a programmable error correcting circuit on said chip;

RAM on said chip storing error correcting information, said RAM being in communication with said programmable error correcting circuit; and wherein:

the programmable error correcting circuit receives said error correcting information and processor instructions containing errors that are not capable of being executed by said processing circuitry, and

said programmable error correcting circuit generates corrected processor instructions in response to said processor instructions containing errors and said error correcting information, the corrected processor instructions being capable of being executed by said processing circuitry.

2. (Canceled)

3. (Previously presented) The processor of claim 1, wherein said error correcting information includes a key that enables selection of error correction specific to an error scheme used to generate said errors.

4. (Original): The processor of claim 1, wherein information provided in compiled computer program data in part controls said error correction, thereby providing complementary error correction with a combination of the error correction key and the information provided in the compiled computer program data.

5-12. (Canceled)

13. (Previously presented)The processor of claim 3, wherein instructions provided to said processor include an intentional introduction of errors which are correctable with error correction algorithms, said correction algorithms pre-selected according to the key.

14-16. (Canceled)

17. (Previously presented) A microprocessor for processing computer programs which are selectively operable on selected ones of individual microprocessors, comprising:

an integrated circuit chip;

instruction processing circuits on said chip;

a programmable error correcting circuit on said chip; and

a memory location for storing error correction information, said programmable error correction circuit selecting an error correction scheme based on said error correction information; and

wherein said programmable error correcting circuit receives instructions having errors and said error correction information, and said instruction processing circuits process corrected instructions generated by said programmable error correcting circuit.

18. (Previously presented) A method for processing a computer programs on a microprocessors, the method comprising:

intentionally placing errors in the computer program;

loading instructions of said computer program onto instruction registers on a microprocessor chip;

storing error correction control information on said chip;

on said chip, correcting said instructions using said error correction control information; and

executing said instructions on said chip.

19-26. (Canceled)